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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/667,226	09/21/2000	KORBIN S. VAN DYKE	5231.27-0052BS	8551

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WILKIE FARR & GALLAGHER LLP
INTELLECTUAL PROPERTY LEGAL ASSISTANTS
787 SEVENTH AVE
NEW YORK, NY 10019-6099

EXAMINER	
COLEMAN, ERIC	
ART UNIT	PAPER NUMBER
2183	6

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/667,226	VAN DYKE ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1 and 35-45* is/are allowed.

6)☒ Claim(s) *2,3,5,8,10,11,13-21,23-26,28-34,46-52,54,56-59,61-65 and 67-71* is/are rejected.

7)☒ Claim(s) *4,6,7,9,12,22,27,53,55,60 and 66* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *No. 3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claim 2,8,10,13-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Phillips (patent No. 6,237,074).

4. Phillips taught the invention as claimed including a data processing ("DP") system comprising:

a) Means and method for decoding and executing instructions of a complex instruction set of a computer the instruction set having variable length instructions and many instructions having multiple side effects (e.g., see col. 6, lines 21-67 and col. 17, lines 48-62); and

b) Means and method for storing information describing the decoding of the complex instructions into architecturally-visible processor registers of the computer (e.g., see col. 3, lines 57-col. 5, line 54 and col. 11, lines 30-65).

5. Philips taught (claims 13-18) decoding information including prefix designation, operand address, immediate value, length of the instruction, instruction pointer and next instruction pointer and intra-instruction pointer value (e.g., see col. 2, lines 1-60). Further (claim 19) since Phillps taught use of the x86 instruction set which comprises plural protection modes it would have been inherent that the decoding of instructions would have had to provide an indication of the protection mode (e.g., see col. 3,lines 7-19).

Claim Rejections - 35 USC § 103

6. Claims 3,5,20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phillips as applied to claims 2,8 above, and further in view of Cheng (patent No. 6,243,804).

7. Cheng taught (claims 3,5,20) recognizing an exception occurring in an instruction after a first side effect of an instruction; transferring control to a software exception handler for the first exception and resuming execution of the excepted instruction after completion of the exception handler, the architecturally-visible processor registers exposing sufficient information (including program counter, accumulator data, CPU status, address pointer to data memory) that the transfer and resumption are effected without saving the full state of the excepted instruction on a memory stack (e.g., see col. 2,line 50-col. 3, line 9).

8. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Phillips and Cheng. One of ordinary skill in the art would have been motivated to incorporate the Cheng teachings of use of shadow registers for storing status data to allow the Phillips system to reduce the time necessary to handle interrupt or exceptions.

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Phillips (patent No. 6,237,074).

10. Phillips taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Means and method for decoding and executing instructions of a complex instruction set of a computer the instruction set having variable length instructions and many instructions having multiple side effects (e.g., see col. 6, lines 21-67 and col. 17, lines 48-62); and

b) Means and method for storing information describing the decoding of the complex instructions into architecturally-visible processor registers of the computer (e.g., see col. 3, lines 57-col. 5, line 54 and col. 11, lines 30-65).

11. As the use of mask register (claims 11) Phillips did not expressly detail this limitation. However, one of ordinary skill implementing the Phillips system that provided interrupts for several classes of instructions of variable lengths would have implemented the selection of exceptions using a mask register to speed selection eliminating the need elaborate decoding to determine the signal that indicated the type of exception.

12. Claims 21,23-26,28,29-34,46-52,55-59,61-65,67-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phillips (patent No. 6,237,074) in view of Cheng (patent No. 6,243,804).

13. Phillips taught the invention as claimed including a data processing ("DP") system comprising:

a) Means and method for decoding and executing instructions of a complex instruction set (claims 50,51, 62) of a computer the instruction set having variable length instructions and many instructions having multiple side effects (e.g., see col. 6, lines 21-67 and col. 17, lines 48-62); and

b) Means and method for storing information describing the decoding of the complex instructions into architecturally-visible processor registers of the computer (e.g., see col. 3, lines 57-col. 5, line 54 and col. 11, lines 30-65).

14. Phiilips taught (claims 29-32) decoding information including prefix designation, operand address, immediate value, length of the instruction, instruction pointer and next instruction pointer and intra-instruction pointer value (e.g., see col. 2, lines 1-60). Further, since Phillips taught use of the x86 instruction set which comprises plural protection modes it would have been inherent that the decoding of instructions would have had to provide an indication of the protection mode (e.g., see col. 3,lines 7-19).

15. Phillips did not specifically disclose the combination of (claims 21,23,24,25,26, 46,47,48,49,52,55-59,61,63,64,65,67-69,71) recognizing an exception occurring in an instruction after a first side effect of an instruction; transferring control to a software

exception handler for the first exception and resuming execution of the excepted instruction after completion of the exception handler, the architecturally-visible processor registers exposing sufficient information (including program counter, accumulator data, CPU status, address pointer to data memory) that the transfer and resumption are effected without saving the full state of the excepted instruction on a memory stack. Cheng however taught his combination of limitations (e.g., see col. 2,line 50-col. 3, line 9). As to the multiple cache levels (claim 48) the use one or more cache levels in systems that implement the x86 instruction set as taught by Phillips was well known in the art. Therefore one of ordinary skill would have used one or more cache levels in implementing the Phillips teachings at least to efficiently ensure that the desired data was available to the processor.

16. As to the further limitation claim 70, It was well known in the art to store instructions in ranges of storages locations. One of ordinary skill would have been motivated to store instruction of different instruction sets in different ranges in memory provide easier control and determination that the correct the of instruction was being fetched as the address would correlate to the type of instruction set.

17. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Phillips and Cheng. One of ordinary skill in the art would have been motivated to incorporate the Cheng teachings of use of shadow registers for storing status data to allow the Phillips system to reduce the time necessary to handle interrupt or exceptions.

18. As per claim 28 one of ordinary skill would have been motivated to abstain from altering the contents of the processor registers during an exception because the Cheng system provided a system that did not save the registers to memory. Therefore to ensure that execution would continue on valid data after return from exception processing the system would have been prevented from altering the processor registers (e.g., see col. 2, lines 50-67 of Cheng).

19. As per claims 33,34, Cheng taught the operation of the exception handler being controlled by the exception handler and storing results in general purpose registers (e.g., see col. 5, lines 3-59).

Allowable Subject Matter

20. Claims 1,35-37,38-45 are allowed.

21. Claims 4,6,7,9,12,22,27,53,54,60,66 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Thomas (patent No. 5,386,563) disclosed a system with register substitution during exception processing (e.g., see abstract).

Garibay (patent No. 5,479,616) disclosed a exception handling for prefetched instruction bytes using valid bits to identify instructions that will cause an exception (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER

June 12, 2004